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1 ECE 637: Digital Integrated Circuits Solution – Sequential Logic Circuits Text: Chapter 7, Digital Integrated Circuits 2 nd Ed, Rabaey 1) i) Draw the schematic for a negative edge triggered D flip-flop using: a. C 2 MOS logic b. TSPC logic Solution:

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Prof. Rabaey has made high-impact contributions to a number of fields, including advanced wireless systems, low power integrated circuits, sensor networks, and ubiquitous computing. His current interests include the conception of the next-generation integrated wireless systems over a broad range of applications, as well as exploring the ...

Jan M. Rabaey | EECS at UC Berkeley

permitted by McGraw-Hill for their individual course preparation. If you are a student using this Manual, The switch in Fig. 7.89 opens at t = 0. Find v 0 for t > 0. Figure 7. For Prob. 7.9. Chapter 7, Solution 9. For t < 0, the switch is closed so that. 4 (0) (6) 4 V 24. vo == + For t >0, we have a source-free RC circuit. 33 τ RC 3 10x x x4 ...

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